Remarks

Reconsideration of this Application is respectfully requested.

Claims 1-6 and 9-12 are pending in the application, with claims 1, 6, and 12 being the independent claims.

Claims 1, 6, and 12 have each been amended to recite that the functional blocks and gate array block are formed on the chip with a single mask. Support for this amendment can be found, for example, on page 4, lines 8-11; page 7, lines 18-21; page 8, lines 4-7; and throughout the specification. (In the disclosure, a non-customized layer is formed by a single common mask which places the functional blocks and gate array block, prior to having electrical connections formed in the gate array block on the surface of the semiconductor chip, and a customized layer is formed by a circuit mask which places electrical connections having desired functions on the gate array block.)

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Based on the above Amendment and the following Remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

1. Claims 1, 5-6 and 12 are rejected under 25 U.S.C. §103(a) as being unpatentable over Andrews et al. (hereinafter "Andrews") and Tavana et al. (hereinafter "Tavana") in view of Kean and Kawashima.

Andrews teaches a hybrid integrated circuit 400 with an array 402 of programmable logic cells (PLC) surrounded on three sides by programmable I/O cells 404 and an outermost ring of pads 406. One side of the PLC array 402 is bounded by field programmable gate array (FPGA) application specific block (ASB) interface hardware 412 that allows the PLC array 402 to interface with an application specific block 408 which can be implemented with mask-programmed devices (MPD)-type logic. (Fig. 4, col. 3, lines 38-48). Thus, Andrews discloses that regions of FPGA-type logic (for example, 402) can be combined with regions of MPD-type logic (for example, 408) on a single chip. (col. 3, lines 7-19). Andrews discloses that the FPGA-type logic can be implemented with "any suitable type of field programmable logic" and that the MPD-type logic an be implemented with "any suitable type of mask-programmable logic." (col. 5, lines 16-23).

Tavana teaches a monolithic circuit device 10 with a field programmable gate array portion 12 and a mask-defined application specific logic area 14. (page 8, lines 17-21 and Fig. 2) Programmable 28 and mask-defined 30 interconnections are used as routing to interconnect the FPGA 12. (page 10, line 12 - page 11, line 2)

Kean teaches a field programmable gate array 10 with a plurality of cells 12 arranged in rows and columns. (see, for example, col. 12, lines 11-26 and Fig 1)

Kawashima teaches a semiconductor integrated circuit, including a technique for increasing the density of integration of input and output buffers in the semiconductor integrated circuit (col. 1, lines 10-17).

<u>The references fail to teach each of the features of the claims.</u>

Each of the independent claims (claims 1, 6, and 12) has been amended to recite that the

functional blocks and the gate array block are formed on the chip with a single mask. None of the cited references teach this feature. As stated above, the primary reference, Andrews, discloses that the FPGA-type logic and the MPD-type logic can be implemented with "any suitable type" of logic. However, there is no disclosure or suggestion that the functional and gate array blocks can be placed on the chip with a single mask. Similarly, the modifying references also fail to teach this feature.

As described on page 10 and throughout the specification, the method recited by the independent claims is advantageous over the prior art because it enables a shorter turn around time for the design and fabrication of the semiconductor chip. The circuit mask for forming circuits in the gate array block can be designed and fabricated in parallel with the design and fabrication of the common mask for forming the functional blocks and gate array block on the surface of the semiconductor chip.

The Office Action fails to set forth a case of *prima facie* obviousness.

Even without a consideration of the teachings of the references and recitations of the claims, the Office Action fails to set forth a case of *prima facie* obviousness to support the rejection. It is initially the Examiner's burden to establish a *prima facie* case of obviousness under 35 U.S.C. §103. If examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more, the applicant is entitled to a grant of a patent. *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443, (Fed. Cir. 1992). To satisfy the Examiner's burden under §103, the Examiner must show some objective teaching in the prior art that would lead one skilled in the art to combine the relevant teachings of the references. *Tec Air, Inc. v. Denso Manufacturing Michigan*, 192 F.3d 1353, 52 USPQ 2d 1294 (Fed. Cir. 1999); *In re Fine*, 837

F.2d 1071, 5 USPQ2d 1596 (Fed Cir. 1988). The absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573, 42 USPQ2d 1378 (Fed. Cir. 1997). As discussed in the following paragraphs, the Examiner fails to set forth a motivation for the proposed combinations of references.

It is not clear whether Tavana is being cited to modify Andrews, the primary reference, or is being cited as an alternative reference for Andrews. If Tavana is being cited to modify Andrews, absolutely no motivation to combine the references is presented. If Tavana is being cited as a primary reference as an alternative to Andrews, then no motivation is set forth to combine Tavana with Kean and/or Kawashima.

The Action cites Kean as teaching that "a field programmable gate array (such as Andrews block 412) has 'basic cells'." However, it fails to set forth a motivation to combine Kean with Andrews.

The Action cites Kawashima as teaching programming field programmable gate array by establishing electrical connections. However, as in the other proposed combinations, it fails to set forth a motivation to combine Kawashima with Andrews.

Because the Office Action fails to set forth a motivation for any of these proposed combinations, then the rejection of each of these claims is improper and should be withdrawn.

2. Claims 2-4 and 9 are rejected under 35 U.S.C. §103(a) as being unpatentable over the references as applied to claims 1, 5-6 and 12, and further in view of Chan et al. (hereinafter "Chan")

Chan teaches routing and logic elements of a field programmable gate array. (see, for example, Fig. 1 and col. 4, lines 36-38)

Like the references discussed above, Chan fails to teach placing the functional blocks and the gate array block on the chip with a single mask. Thus, Chan fails to bridge the deficiency in the rejection of the independent claims.

The Office Action cites Chan as teaching that application specific circuits can be designed with gate array, standard cell, full custom, and programmable logic devices. The Examiner states that "any of these techniques would have been obvious, because each technique is known in the art, and therefore has known advantages, and because each of the techniques is an alternative to the other." However, this statement does not provide a motivation to combine the cited references. A statement that the techniques have advantages or that the techniques are alternatives to each other does not supply any motivation to combine the particular teachings of Chan with the particular teachings disclosed in Andrews.

3. Claims 10-11 are rejected under 35 U.S.C. §103(a) as being unpatentable over the references as applied to claims 1, 5-6 and 12, and further in view of Dangelo.

Dangelo teaches arrangements and interconnections of cores on a silicon substrate. (see, for example, Figs. 1 and 2). The cores may include CPU 102 and memory 108. (col. 3, lines 51-53 and col. 4, lines 10-11).

However, Dangelo fails to teach that the gate array block and functional blocks can be formed using a common mask. Thus, Dangelo fails to bridge the deficiency in the rejection of the independent claims.

4. Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner

reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance with claims 1-6 and 9-12.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

Date: 12/13/01

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Version With Markings To Show Changes Made

In The Specification:

Please amend the specification as follows:

Page 6, replace the paragraph beginning on line 19 with the following rewritten paragraph:

It is desirable to adopt the standard cell system or full custom system as described above for the purpose of reducing the area of an IC chip. As has been practiced by the embedded array system in general, a single common mask used for the formation of each non-customized layer is designed and manufactured prior to (or in parallel with) the formation of a customized layer so that the TAT can be shortened.

Pages 6, replace the paragraph beginning on line 26 with the following rewritten paragraph:

In order to previously design and manufacture the common mask for the non-customized layer, the following two conditions must be met. The first condition is as follows: It is necessary to fix patterns for functional elements or devices such as transistors for constituting each non-customized layer and avoid changes in patterns after the design and fabrication of the mask are started. Further, the second condition is as follows: Interconnections in each wiring layer used as a customized layer are suitably formed in association with the non-customized layer so that desired functions are obtained. Namely, if basic gates (also called "basic cells") based on the gate array system are partially embedded in the IC designed by the standard cell system or full custom system, and the plurality of embedded basic gates are electrically connected to one another and utilized in combination so as to implement the desired functions, then the common mask used for the non-customized layer can be designed and fabricated prior to the formation of

the customized layer even in the case of the IC designed by the standard cell system or full custom system.

Page 7, replace the paragraph beginning on line 17 with the following rewritten paragraph:

A process for designing such an IC as to allow the common mask for the non-customized layer to be designed and fabricated prior to the formation of the customized layer, using the standard cell system or full custom system will next be explained.

Pages 7, replace the paragraph beginning on line 28 with the following rewritten paragraph:

Next, design resources based on the gate array system are blocked to effect layout design on the area having the potential of change in circuit. The layout of the entire IC is designed while the blocked design resources based on the gate array system are being captured by a CAD (Computer Aided Design) of the standard cell system or full custom system. Upon completion of the layout design of the entire IC, the design and fabrication of the common mask related to the non-customized layer is started.

Page 8, replace the paragraph beginning on line 8 with the following rewritten paragraph:

Thereafter, when the contents of the circuit is determined in the area having the potential of the change in circuit, each gate array block corresponding to a basic cell block is again laid out using the CAD of the gate array system. The design and fabrication of [the] a circuit mask corresponding to each customized layer are started based on the re-laid out gate array block. Incidentally, the gate array block whose circuit has been determined, is laid-out in a design based on the non-customized layer formed by the previously-designed and fabricated common mask. Namely, the gate array block preceding the determination of the circuit and the gate array block subsequent to the determination of the circuit are respectively made up of the same basic gate comprised of basic gates identical in number in both the vertical and horizontal directions.

Page 10, replace the paragraph beginning on line 4 with the following rewritten paragraph:

Since diffused layers, polysilicon layers, metal wiring layers, etc. are conventionally formed after the design and fabrication of the masks when the IC is designed by the standard cell system or full custom system, it normally took several months to complete the IC. On the other hand, according to the IC chip 1 in an embodiment of the present invention, it is possible to previously design and manufacture the common mask corresponding to the non-customized layer during a logic-simulation stage, for example. Further, the design work such as the logic simulation or the like is continuously performed in parallel with the design and fabrication of the common mask. Thereafter, when the corresponding circuit for the gate array block 34 has been determined, the layout of the gate array block 34 is designed again, and [a] the circuit mask corresponding to a customized layer is designed fabricated.

Page 11, replace the paragraph beginning on line 1 with the following rewritten paragraph:

According to the IC chip 1 related to the embodiment of the present invention, when a circuit change occurs in the gate array block 34, the designer of the IC chip can cope with such a circuit change by redesigning only the gate array block 34 while the contents of the circuit of the non-customized layer is maintained. That is, only the circuit mask related to the gate array block 34 is changed in design. Thus, the circuit change of the gate array block 34 can be completed in a short period of time.

In the Claims:

Please amend claims 1, 6, and 12 as follows:

1. (Thrice Amended) A method of manufacturing a semiconductor integrated circuit comprised of a plurality of functional blocks and a gate array block, each of the plurality of functional blocks being respectively provided with predetermined functions by semiconductor devices, the method comprising the steps of:

placing the gate array block comprised of a plurality of basic cells arranged in line and the plurality of functional blocks within a predetermined first area including a center position on a surface of a semiconductor chip, the gate array block and the plurality of functional blocks being formed on the surface of the semiconductor chip with a common mask;

placing a plurality of I/O buffers in a second area surrounding the first area;

designing circuits for inclusion in the gate array block; and

establishing electrical connections between the basic cells within the gate array block by using interconnections according to the circuits designed in the previous step.

6. (Thrice Amended) A semiconductor integrated circuit comprising:

a plurality of functional blocks placed on a semiconductor chip, said functional blocks being respectively provided with predetermined functions by semiconductor devices;

a gate array block placed on said chip, said gate array block being comprised of a plurality of basic cells arranged in line and electrically connected between the basic cells lying within the gate array block by interconnections implementing a desired function, the gate array block having a circuit designed after placing said plurality of functional blocks and said plurality of basic cells on said chip,

wherein said functional blocks and said gate array block are laid out with a common mask in a first area including a center position on a surface of the semiconductor chip; and

a plurality of I/O buffers surrounding the first area.

12. (Twice Amended) A method of manufacturing a semiconductor integrated circuit comprising a plurality of functional blocks and a gate array block, each of said plurality of functional blocks being respectively completed by a layout design, the method comprising the steps of :

placing the gate array block, comprised of a plurality of basic cells arranged in line, within a first area of a semiconductor chip and said plurality of functional blocks within a second area of said semiconductor chip, the gate array block and the plurality of functional blocks being formed on the surface of the semiconductor chip with a common mask;

placing a plurality of I/O buffers in a third area surrounding the first and second areas;

designing circuits for inclusion in the gate array block; and

establishing electrical connections between the basic cells lying within the gate array block by using interconnections in accordance with the designed circuits whereby said designed circuits are formed on said semiconductor chip.